WHAT IS CLAIMED IS:

1. A method for forming a planarized layer of material on a processed wafer, the wafer having a top surface, the top surface having a wafer lower level and a wafer upper level that lies above the wafer lower level, the method comprising the steps of:

forming a layer of first material on the top surface of the wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level;

forming a layer of second material on the top surface of the layer of second material; and

chemically-mechanically polishing the layer of second material and the underlying layer of first material until the layer of second material is all removed from the layer of first material to form the planarized layer of material.

2. The method of claim 1 wherein the first lower level lies above the wafer upper level.

3. The method of claim 2 and further comprising the step of etching the planarized layer of material to form a structure.

4. The method of claim 3 wherein the structure has a thickness that ranges from a minimum thickness to a maximum thickness over the wafer upper level.

5. The method of claim 4 wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a value that is equal to or greater than the minimum thickness.

6. The method of claim 1 wherein the first material is polysilicon.

7. The method of claim 1 wherein the second material is oxide.

8. The method of claim 1 wherein the structure is a local interconnect line.

9. The method of claim 1 wherein the first and second layers of material are chemically-mechanically polished with a slurry that has a selectivity that falls within an approximate range of 0.9-1.1:1.

10. The method of claim 2 and further comprising the step of forming a layer of third material on the planarized layer of material.

11. The method of claim 10 and further comprising the step of etching the layer of third material and the planarized layer of material to form a structure.

12. The method of claim 11 wherein the structure has a thickness that ranges from a minimum thickness to a maximum thickness over the wafer upper level.

13. The method of claim 12 wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a value that is equal to or greater than the minimum thickness.

14. The method of claim 1 and further comprising the step of doping the layer of first material prior to forming the layer of second material.

15. The method of claim 1 wherein the layer of first material is doped polysilicon.

16. The method of claim 3 wherein the layer of first material makes an electrical contact with a device on the wafer.

17. The method of claim 1 wherein the layer of second material is approximately two to three times as thick as the layer of first material.